

IN THE SPECIFICATION:

Please replace paragraph number [0001] with the following rewritten paragraph:

[0001] This application is a continuation of application Serial No. 09/920,253, filed August 1, 2001, ~~pending~~ now U.S. Patent 6,616,880, issued on September 9, 2003, which is a continuation of application Serial No. 09/481,166, filed January 12, 2000, now U.S. Patent 6,287,503, issued September 11, 2001, which is a continuation of application Serial No. 09/019,226, filed February 5, 1998, now U.S. Patent No. 6,117,382, issued September 12, 2000.

Please replace paragraph number [0003] with the following rewritten paragraph:

[0003] State of the Art: Modern packaged integrated circuits (IC) comprise one or more encased semiconductor devices or chips within a protective "package" of plastic, ceramic, moldable material, or metal or other preformed material, such as caps. The integrated circuit chips are made from a semiconductor material such as silicon, germanium or gallium arsenide, and microscopic circuits are formed on a surface of each chip surface by photolithographic techniques. A plurality of external connections, typically designed for soldering or slide connections, are connected to bond pads on one or more encased chips, enabling the chips to be electrically interconnected to an external electrical apparatus. In one form of interconnection, a substrate such as a wiring board or circuit board has an array of conductors which is typically connected to the wire bond pads of the chips. Portions of the conductors extend through the substrate, typically in through-holes or vias to the opposite side for conductive, ~~e.g.~~ e.g., solder, connection to another electronic apparatus. In addition to one or more semiconductor devices (chips or dies) attached to the substrate, or in lieu thereof, other devices such as resistors, capacitors, etc., as well as the conductive leads and wires, may be mounted to the substrate and incorporated in the circuit. Such elements are encased in plastic, ceramic or other material for protection.

Please replace paragraph number [0004] with the following rewritten paragraph:

[0004] Plastic encapsulation of semiconductor and other electronic devices by transfer molding is a well-known and much-used technique. Typically, a large number of components or devices is placed in a lower mold plate or half of an open multi-cavity mold, one device within each cavity. The mold is closed with a mating upper plate. The cavities of the mold are connected by tiny “~~feed-runners~~”, runners,”~~i.e.~~ i.e., channels to a “pot” or reservoir from which pressurized liquified plastic is fed. Typically, a constricted channel known as a “gate” is located at the entrance to each mold cavity to limit the flow rate and injection velocity of liquified plastic into the cavity.

Please replace paragraph number [0006] with the following rewritten paragraph:

[0006] Typically, powdered or pelletized plastic, ~~e.g.~~ e.g., thermoset resin, is placed in the resin pot and pressed by a ram. The heated, pressurized plastic becomes liquified and flows through the feed runners and gates to surround each device on one side of the substrate and fill that portion of each mold cavity, where it subsequently hardens to encapsulate one side of the board and the devices attached to it. Air is expelled from each cavity through one or more vent runners as the plastic melt fills the mold cavities. Following hardening by partial cure of the thermoset plastic, the mold plates are separated along the parting line and each encapsulated device is removed from a mold cavity and trimmed of excess plastic which has solidified in the runners and gates. Additional thermal treatment completes curing of the plastic package.

Please replace paragraph number [0007] with the following rewritten paragraph:

[0007] Following removal of each encased unit from its mold cavity and curing, the peripheral portions of the board may be excised from the board and any flash,~~i.e.~~ i.e., plastic or other extraneous material removed from external terminals, etc. as known in the art, and the device is ready for use.

Please replace paragraph number [0008] with the following rewritten paragraph:

[0008] In devices having one side of the substrate configured for a ~~ball-grid~~ ball-grid-array (BGA) or similar array on a circuit board, the molding process is conducted so that the surface of the circuit board having the ~~ball-grid~~ ball-grid-array connections are formed on an outer surface of the package, such surface not being covered or encapsulated by the plastic material during the encapsulation process. When the substrate is sealably clamped on all sides of the cavity, plastic may reach the ~~ball-grid~~ ball-grid-array side of the substrate only through the substrate, ~~e.g. e.g.~~, inadvertently through a hole or via. Of course, following removal from the cavity, any plastic encapsulant which may have reached and solidified on the ~~ball-grid~~ ball-grid-array connection surface is removed.

Please replace paragraph number [0017] with the following rewritten paragraph:

[0017] The invention comprises an improved method and apparatus for encapsulating or enclosing electronic devices mounted on the first side of a substrate such as a circuit board or wiring board. The invention may be particularly applied to one-side encapsulation or enclosing of electronic devices which includes a substrate such as a circuit board configured to have a ~~ball~~ ball-grid-array (BGA), pin-grid\_array (PGA), land-grid-array (LGA) or similar set of multiple electrical terminals on its opposite side. The ~~array~~ array of terminals of such a substrate is typically configured to be bonded to terminals of another apparatus following encapsulation of the electronic devices including IC chip(s), leads, wiring and/or other components on its first side with plastic.

Please replace paragraph number [0019] with the following rewritten paragraph:

[0019] In the invention, a pair of mold plates is modified from a conventional configuration so that two array packages may be simultaneously encapsulated, ~~back-to~~ back-to-back, within a single mold cavity. Thus, the number of packages encapsulated in a mold machine may be doubled without any significant increase in packaging cycle time.

Please replace paragraph number [0022] with the following rewritten paragraph:

[0022] The method is applicable to a wide variety of substrate-based conductor-~~grid-~~grid-array packages, including those mounted on monolayer substrates, multi-layer circuit board substrates, multi-chip-modules (MCM), etc. The production rate is effectively doubled, and encapsulation of devices with different substrate thicknesses may be performed without adjustment of the mold plate spacing.

Please replace paragraph number [0037] with the following rewritten paragraph:

[0037] A method for rapid one-side encasing of array packages and an apparatus for performing such packaging are described. The several aspects of the invention are particularly applicable to substrate-mounted arrays of ball grids, pin grids and ~~land-~~ land grids with various encapsulable devices mounted on the opposite side of the substrate. In addition, devices having exposed heat sinks or heat radiators on the opposite side of an otherwise impermeable substrate may be rapidly one-side encapsulated by the method and apparatus of the invention. The method and apparatus are applicable to any device including a generally planar substrate, wherein one side of the substrate is to be non-encapsulated in the final packaged form.

Please replace paragraph number [0041] with the following rewritten paragraph:

[0041] The lower mold plate 14 is typically ~~a substantially~~ a substantially a mirror image of the upper mold plate 12, although it does not need to be such a mirror image, having lower cavity portion 16B which mates with the upper cavity portion 16A. Thus, the upper cavity portion 16A and mating lower cavity portion 16B together comprise a complete mold cavity 16. Each lower cavity portion 16B has a lower feed runner 34 with gate 36 along upper flat surface 22 for injecting a second fluid plastic 40 into each lower cavity portion at a controlled rate. Although the fluid plastics 30 and 40 may usually be the same material, encapsulants of differing composition may be used as described herein, infra. In addition, although the first fluid plastic 30 and second fluid plastic 40 are typically injected simultaneously, they may alternatively

be injected in sequence, particularly if they differ. Lower vent runner 38 for venting gas, etc., from lower cavity portion 16B during encapsulation is shown.

Please replace paragraph number [0044] with the following rewritten paragraph:

[0044] The upper mold plate 12 generally has a flat upper surface 42, and the lower mold plate 14 has a flat lower surface 44. Following placement of the devices 50A, 50B back-to-back between the mold plates 12, 14, compressive forces 46 are exerted upon surfaces 42, 44 to clamp the mold plates 12, 14 against the pair of substrates 18A, 18B, and the encapsulation process may proceed without leakage. The array of terminals is configured to be positioned outside of the area under high compression to avoid damage to the terminals. Thus, the area under compression is “circumferential” about each cavity, where “circumferential” refers to the excluded area rather than any circularity. The cavities are usually rectangular in shape rather than round.

Please replace paragraph number [0045] with the following rewritten paragraph:

[0045] Although the surfaces 20, 22 of the upper mold plate 12 and lower mold plate 14, respectively, are shown in FIG. 1 as planar, one or both of the surfaces 20, 22 may incorporate projecting ridges by which the compressive forces 46 are concentrated over a relatively small area of the substrates 18A, 18B. If this is done, the terminals of the array may be both inside and outside of the circumferential ridge about a mold cavity portion 16A or 16B or both.

Please replace paragraph number [0049] with the following rewritten paragraph:

[0049] First, buffer members 60 of differing thicknesses may be readily provided for encapsulation of packages having varying substrate thicknesses 58A, 58B (see FIG. 2). For example, when a pair of electronic devices 50A, 50B having a reduced substrate thickness 58A and/or 58B is to be one-side encapsulated, a buffer member 60 of greater thickness-dimension 68 may be used to compensate for the thinner substrates 18A, 18B. The tedious adjustment of the

molding machine 10 for a different mold plate clearance to accommodate varying substrate thicknesses 58A, 58B may be avoided.

Please replace paragraph number [0051] with the following rewritten paragraph:

[0051] Third, the buffer member 60 may be adapted to accommodate projecting array terminals such as ~~pin-grid~~ grid-arrays and ball-grid-arrays, etc., preventing damage to the pins or solder balls resulting from compression against the opposite substrate or the buffer member 60 itself.

Please replace paragraph number [0055] with the following rewritten paragraph:

[0055] In FIG. 5, the molding plates of FIG. 1 are shown in a method for one-side encapsulation of a pair of typical electronic devices 50A and 50B, each comprising components 52A, ~~54A~~ (or 52B, ~~54B~~) mounted on a substrate 18A (or 18B) such as a circuit board with a ball-grid-array of solder balls 62A, 62B, respectively. The electronic devices 50A, 50B are placed back-to-back in the mold cavity 16, with an intervening buffer member 60. The substrates and buffer member 60 form a "laminar" arrangement, though they are not attached to each other. As depicted in FIGS. 5 and 6, the buffer member 60 includes ~~cut-outs~~ cut-outs 64 and 66, ~~respectively~~, into which the arrays of solder balls 62A and 62B are positioned. The thickness 68 of the buffer member 60 in a compressed condition enables the solder balls 62A, 62B from both substrates 18A, 18B to fit within the ~~cut-outs~~ cut-outs 64, ~~66~~ without touching, so that deformation or damage to the solder balls is avoided. For typical ball-grid-arrays (BGA), the thickness 68 of the buffer member 60 will be sufficient to accommodate both sets of solder balls 62A, 62B. Where used for pin-grid-arrays (PGA), the required thickness will vary depending upon pin length.

Please replace paragraph number [0057] with the following rewritten paragraph:

[0057] As already indicated, this method is shown in FIG. 5 for devices with ~~ball-grid~~ grid-arrays (BGA). The method shown in FIG. 5 is equally useful for substrates in which a

pin-grid-array (PGA) or land-grid-array (LGA), etc., or others, with pads having already been provided in the substrate.

Please replace paragraph number [0058] with the following rewritten paragraph:

[0058] The cut-out 64 ~~and 66~~ may be made in the buffer member 60 by any feasible method, including stamping or laser cutting.

Please replace paragraph number [0059] with the following rewritten paragraph:

[0059] FIGS. 7 and 8 illustrate a further embodiment of the invention. The buffer member 60 is perforated with groupings 70 of cut-outs 66 to accommodate array pads, balls, pins, etc. which protrude from the bare substrate second sides 56A, 56B and which otherwise would impinge on both parallel surfaces 72A, 72B of the buffer member. The cut-outs 66 are aligned with the conductors and are of such a size to accommodate the usual variability in positioning of the substrates 18A, 18B on the buffer member 60. The cut-outs 66 in the buffer member 60 may be formed by any method capable of forming small holes, including laser cutting or ~~“drilling”~~, “drilling,” and extend from the upper surface 72A to the lower surface 72B.

Please replace paragraph number [0061] with the following rewritten paragraph:

[0061] The buffer member 60 may typically be re-used more than once, and may be ~~usable~~ used repeatedly, thus saving time and materials.

Please replace paragraph number [0065] with the following rewritten paragraph:

[0065] The upper plate 112 is shown as similar to a conventional, generally rectangular plate member with multiple upper cavity portions 116A along its face, ~~i.e.~~ i.e., lower flat surface 120. Each upper cavity portion 116A has an aperture 126 therein connected to a source of vacuum.

Please replace paragraph number [0066] with the following rewritten paragraph:

[0066] The lower plate 114 is ~~a substantially~~ substantially a mirror image, although not required, of the upper plate 112, having lower cavity portion 116B along its face, i.e., upper flat surface 122, which mates with the upper cavity portion 116A. Thus, the upper cavity portion 116A and mating lower cavity portion 116B together comprise a complete cavity 116. Each lower cavity portion 116B has an aperture 126 therein connected to a source of vacuum.

Please replace paragraph number [0067] with the following rewritten paragraph:

[0067] In accordance with the invention, two electronic devices 50A and 50B are shown within the cavity 116, in a back-to-back orientation, the substrate second sides 56A and 56B, respectively, in abutment. Upper device 50A comprises a planar substrate 18A having a first side 48A upon which a semiconductor die component 52A is attached and electrically connected thereto by wires 54A or some other suitable connection. Likewise, lower device 50B is shown as comprising a planar substrate 18B having a first side 48B upon which a semiconductor die component 52B is attached and electrically connected via wires 54B. The first and second devices 50A, 50B may each have an array of conductive terminals, e.g. pads, not visible, on substrate second side 56A or 56B, respectively, each array of terminals connected by conductors (not shown) passing through the respective substrate 18A or 18B to the wires 54A, 54B of the device.

Please replace paragraph number [0068] with the following rewritten paragraph:

[0068] Contained within upper cavity portion 116A of upper plate 112 is a cover 130 being held therein through the use of a vacuum supplied through aperture 126 after being placed therein in any suitable manner. Similarly, contained within lower cavity portion 116B of lower plate 114 is a cover 130 being held therein through the use of a vacuum supplied through aperture 126 after being placed therein in any suitable manner. The covers 130 may be of any type of suitable material in any suitable shape for application to the substrate 18A or 18B to encase the semiconductor die component 52A and ~~52B~~ 52B, respectively.

Please replace paragraph number [0070] with the following rewritten paragraph:

[0070] The upper plate 112 generally has a flat upper surface 142, and the lower plate 114 has a flat lower surface 144. Following placement of the electronic devices 50A, 50B back-to-back between the plates 112, 114, compressive forces 46 are exerted upon surfaces 142, 144 to clamp the plates 112, 114 against the pair of substrates 18A, 18B and the process proceeds to attach, such as by using adhesive bonding, the covers 130 to the substrate 18A, 18B. The lower edge of each cover 130 may be coated with a suitable adhesive to attach the cover 130 to the substrate 18A, 18B. The wire bonds to the circuits of the substrate 18A, 18B are placed to be located outside the area of compression of the edge of the cover 130 on the substrate 18A, 18B. As stated, the cover 130 may be of any shape desired to enclose and isolate a desired area on the substrate 18A, 18B.

Please replace paragraph number [0071] with the following rewritten paragraph:

[0071] Referring to FIG. 10, another embodiment of the present invention is shown such as illustrated in FIG. 9, except that each cover 130 has the lower edge thereof secured in a recess 18C or 18D formed in substrate 18A, 18B ~~respectively~~, respectively. The lower edge of cover 130 may be secured in the recess 18C, 18D of substrate 18A, 18B, respectively, by means of a suitable adhesive or any other suitable, well-known attachment.

Please replace paragraph number [0072] with the following rewritten paragraph:

[0072] Referring to FIG. 11, another embodiment of the present invention is shown wherein the plates of FIG. 9 are used for one-side encapsulation of a pair of typical electronic devices 50A and 50B, each comprising components 52A, ~~54A~~ (or 52B, ~~54B~~) mounted on a substrate 18A (or 18B) such as a circuit board with a ball-grid-array of solder balls 62A, 62B, respectively. The devices 50A, 50B are placed back-to-back in the mold cavity 116, with an intervening buffer member 60. The substrates and buffer member 60 form a "laminar" arrangement, though they are not attached to each other. As depicted in FIGS. 11 and 5, the

buffer member 60 includes a cut-out 64 ~~and 66, respectively,~~ into which the arrays of solder balls 62A and 62B are positioned. The thickness 68 of the buffer member 60 in a compressed condition enables the solder balls 62A, 62B from both substrates 18A, 18B to fit within the ~~cut-~~ cut-outs 64, 66 (shown in FIG. 12) without touching, so that deformation or damage to the solder balls is avoided. The cover 130 is attached to substrate 18A, 18B by any suitable arrangement, such as adhesive bonding, etc.